CLAIMS:

1. A semiconductor device comprising:

a first transistor having a composite gate structure containing a lamination of a first polycrystalline silicon film, an interlayer insulating film, and a second polycrystalline silicon film; and

a second transistor having a single gate structure containing a lamination of a third polycrystalline silicon film and a fourth polycrystalline silicon film:

wherein said first polycrystalline silicon film and said third polycrystalline silicon film have substantially the same thickness, and said first polycrystalline silicon film and said third polycrystalline silicon film have different impurity concentrations independently controlled of each other; and

said second polycrystalline silicon film and said fourth polycrystalline silicon film have substantially the same thickness, and said second polycrystalline silicon film, said fourth polycrystalline silicon film, and also said third polycrystalline silicon film have substantially the same impurity concentration.

2. A semiconductor device as claimed in claim 1, wherein the impurity concentration of said first polycrystalline silicon film is 1×10^{18} to 1×10^{19} atoms/cm^3, and the impurity concentration of said third polycrystalline silicon film is 1×10^{20} to 1×10^{21} atoms/cm^3.

3. A semiconductor device as claimed in claim 1,

wherein said interlayer insulating film is a multilayer insulating film containing a silicon nitride film.

4. A semiconductor device as claimed in claim 1, wherein said first transistor is a nonvolatile semiconductor element, and said second transistor is an MOS transistor.

5. A semiconductor device as claimed in claim 1, further comprising an insulating film formed just above said fourth polycrystalline silicon film of said second transistor, a contact hole formed to penetrate at least said insulating film and a wiring layer formed on said insulating film and electrically connected through said contact hole to said fourth polycrystalline silicon film.

6. A semiconductor device comprising:

a first transistor having a composite gate structure containing a lamination of a first polycrystalline silicon film, an interlayer insulating film, and a second polycrystalline silicon film;

a second transistor having a single gate structure containing a lamination of a third polycrystalline silicon film, an interlayer insulating film, and a fourth polycrystalline silicon film; and

an extension of a lamination of said third and fourth polycrystalline silicon films functioning as a wiring of said gate electrode of said second transistor;

wherein said first polycrystalline silicon film and said third polycrystalline silicon film have substantially the same thickness; and said first polycrystalline

silicon film, and said third polycrystalline silicon film included in said extension of the lamination of said third and fourth polycrystalline silicon films have different impurity concentrations controlled independently of each other; and

said second polycrystalline silicon film and said fourth polycrystalline silicon film have substantially the same thickness; and the impurity concentration of said second polycrystalline silicon film is substantially equal to the impurity concentration of said third polycrystalline silicon film included in said extension of the lamination of said third and fourth polycrystalline silicon films.

7. A semiconductor device as claimed in claim 6, wherein the impurity concentration of said first polycrystalline silicon film is 1×10^{18} to 1×10^{19} atoms/cm^3, and the impurity concentration of said third polycrystalline silicon film included in said extension of the lamination of said third and fourth polycrystalline silicon films is 1×10^{20} to 1×10^{21} atoms/cm^3.

8. A semiconductor device as claimed in claim 6, wherein said interlayer insulating film is a multilayer insulating film containing a silicon nitride film.

9. A semiconductor device as claimed in claim 6, wherein said first transistor is a nonvolatile semiconductor element, and said second transistor is an MOS transistor.

10. A semiconductor device as claimed in claim 6,

further comprising an insulating film formed just above said fourth polycrystalline silicon film of said second transistor, a contact hole formed to penetrate at least said insulating film and a wiring layer formed on said insulating film and electrically connected through said contact hole to said fourth polycrystalline silicon film.

11. A method for manufacturing a semiconductor device including a first transistor having a composite gate structure and a second transistor having a single gate structure, said method comprising the steps of:

forming a first insulating film on a surface of a first region of a semiconductor substrate and forming a second insulating film on a surface of a second region of said semiconductor substrate;

forming a first polycrystalline silicon film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first polycrystalline silicon film by ion injection;

patterning said first polycrystalline silicon film into a predetermined shape in said first region;

forming a third insulating film containing at least a silicon nitride film on at least said first region except for said second region of said semiconductor substrate;

forming a second polycrystalline silicon film over the entire surface of said semiconductor substrate;

introducing an impurity at a second

predetermined concentration higher than said first concentration into said second polycrystalline silicon film by thermal diffusion; and

patterning a lamination of said second polycrystalline silicon film, said third insulating film and said first polycrystalline silicon film into a predetermined shape in said first region thereby forming said composite gate structure of said first transistor and a lamination of said first polycrystalline silicon film and said second polycrystalline silicon film into a predetermined shape in said second region thereby forming said single gate structure of said second transistor.

12. A method as claimed in claim 11, wherein said first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3, and said second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

13. A method as claimed in claim 11 wherein said third insulating film is an ONO film containing a silicon oxide film, a silicon nitride film and a silicon oxide film.

14. A method for manufacturing a semiconductor device including a first transistor having a composite gate structure and a second transistor having a single gate structure, said method comprising the steps of:

forming a first insulating film on a surface of an active region of a first region of a semiconductor substrate and forming a second insulating film on a surface of an active region of a second region of the

semiconductor substrate;

forming a first polycrystalline silicon film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first polycrystalline silicon film by ion injection;

patterning said first polycrystalline silicon film into a predetermined shape in said active region of the first region;

forming a third insulating film containing at least a silicon nitride film on at least said first region and said active region of the second region except for an element isolation region of said second region of said semiconductor substrate;

forming a second polycrystalline silicon film over the entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first concentration into said second polycrystalline silicon film by thermal diffusion method; and

patterning a lamination of said second polycrystalline silicon film, said third insulating film, and said first polycrystalline silicon film into a predetermined shape in said active region of the first region thereby forming said composite gate structure of said first transistor; and a lamination of said first polycrystalline silicon film, said third insulating film and said second polycrystalline silicon film into a

predetermined shape in said active region of the second region thereby forming said single gate structure of said second transistor.

15. A method as claimed in claim 14, wherein said first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3, and the second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

16. A method as claimed in claim 14, wherein: said third insulating film is an ONO film containing a silicon oxide film, a silicon nitride film, and a silicon oxide film.

17. A method as claimed in claim 14, further comprising the steps of forming an interlayer insulating film just above said second polycrystalline silicon film in said active region of said second region, forming a contact hole to penetrate at least said interlayer insulating film and forming a wiring layer on said interlayer insulating film so as to be connected through said control hole to said second polycrystalline silicon film.

18. A semiconductor device comprising:

a first transistor having a composite gate structure containing a first conductive film, an insulating film, and a second conductive film; and

a second transistor having a single gate structure containing a third conductive film;

wherein said second conductive film and said third conductive film have substantially the same

conductivity;

said third conductive film has a thickness substantially the same as a total of a thickness of said first conductive film and a thickness of said second conductive film; and

said first conductive film has a conductivity different from the conductivity of any of said second conductive film and said third conductive film.

19. A semiconductor device as claimed in claim 18, wherein said third conductive film contains a multilayer conductive film.

20. A semiconductor device as claimed in claim 19, wherein: said first conductive film contains a first silicon film, said second conductive film contains a second silicon film, and said third conductive film contains third and fourth silicon films.

21. A semiconductor device as claimed in claim 20, wherein said first silicon film contains an impurity at an impurity concentration of 1×10^{18} to 1×10^{19} atoms/cm^3, and each of said second, third, and fourth silicon films contains an impurity at an impurity concentration of 1×10^{20} to 1×10^{21} atoms/cm^3.

22. A semiconductor device as claimed in claim 18, wherein said insulating film contains a nitride film.

23. A semiconductor device as claimed in claim 18, wherein said insulating film is a multilayer insulating film containing at least an oxide film and a nitride film.

24. A semiconductor device as claimed in claim 18, wherein said first transistor is a nonvolatile semiconductor memory element, and said second transistor is an MOS transistor.

25. A semiconductor device as claimed in claim 18, wherein said second transistor is formed in an active region surrounded by an element isolation region; and said third conductive film contains a lamination of at least a fourth conductive layer and a fifth conductive layer such that said fourth conductive film is opposing to said fifth conductive film with an insulating film interposed therebetween in said active region; and

the lamination of said fourth conductive film and said fifth conductive film extends over said element isolation region and said fourth and fifth conductive films are in face-to-face contact with each other in said element isolation region.

26. A semiconductor device as claimed in claim 25, wherein said fifth conductive film is formed just over an enter surface of said fourth conductive film.

27. A semiconductor device as claimed in claim 25, wherein said first conductive film contains a first silicon film and said second conductive film contains third and fourth silicon films.

28. A semiconductor device as claimed in claim 25, wherein said insulating film is formed just over an entire surface of said fourth conductive film and said fifth conductive film is formed just over an entire

surface of said insulating film.

29. A semiconductor device as claimed in claim 18, wherein said first conductive film is formed on a second insulating film, which is formed on a surface of a first active region of a semiconductor substrate; said first conductive film, said first-mentioned insulating film, and said second conductive film are patterned into a shape of said composite gate structure of said first transistor in said first active region; said third conductive film is formed on a third insulating film, which is formed on a surface of a second active region of said semiconductor substrate, and is patterned into a shape of said single gate structure of said second transistor in said second active region; and

said semiconductor device further comprises:

drain/source regions of said first transistor formed in said first active region at both sides of said first conductive film, which has been patterned into the shape of said composite gate structure of said first transistor; and

drain/source regions of said second transistor formed in said second active region at both sides of said third conductive film which has been patterned into the shape of said single gate structure of said second transistor.

30. A semiconductor device as claimed in claim 25, further comprising an interlayer insulating film formed just above at least said fifth conductive film of said

second transistor, a contact hole formed to penetrate at least said interlayer insulating film and a wiring layer formed on said interlayer insulating film and electrically connected through said contact hole to said fifth conductive film.

31. A method for manufacturing a semiconductor device including a first transistor having a composite gate structure and a second transistor having a single gate structure, said method comprising the steps of:

forming a first insulating film on a surface of an active region in a first region of a semiconductor substrate and forming a second insulating film on a surface of an active region in a second region of said semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a third insulating film above said first conductive film at least on said first region except for said second region;

forming a conductive film over the entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said second conductive film, said third insulating film, and said first conductive film into a predetermined shape in said first region thereby forming said composite gate structure of said first transistor; and a lamination of said first conductive film and said second conductive film into a predetermined shape in said second region thereby forming said single gate structure of said second transistor.

32. A method as claimed in claim 31, wherein said third insulating film includes a nitride film.

33. A method as claimed in claim 31, wherein said third insulating film is a multilayer insulating film containing at least an oxide film and a nitride film.

34. A method as claimed in claim 31, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

35. A method as claimed in claim 34, wherein said first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3, and said second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

36. A method for manufacturing a semiconductor device including a first transistor having a composite gate structure and a second transistor having a single gate structure, said method comprising the steps of:

forming a first insulating film on a surface of an active region in a first region of a semiconductor substrate and forming a second insulating film on a

surface of an active region in a second region of said semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a third insulating film above said first conductive film, on at least said first region and the active region of said second region except for an element isolation region of said second region;

forming a second conductive film over the entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said second conductive film, said third insulating film and said first conductive film into a predetermined shape in the active region of said first region thereby forming said composite gate structure of said first transistor; and a lamination of said first conductive film, said third insulating film and said second conductive film into a predetermined shape in said second region thereby forming said single gate structure of said second transistor.

37. A method as claimed in claim 36, wherein said step of forming the single gate structure of said second

transistor includes a substep of patterning the lamination of said second conductive film, said third insulating film and said first conductive film into a predetermined shape in the active region of said second region; and patterning a lamination of said second conductive film and said first conductive film into a predetermined shape in said element isolating region of said second region.

38. A method as claimed in claim 36, wherein said third insulating film includes a nitride film.

39. A method as claimed in claim 36, wherein said third insulating film is a multilayer insulating film containing at least an oxide film and a nitride film.

40. A method as claimed in claim 36, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

41. A method as claimed in claim 36, wherein said first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3, and said second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

42. A method as claimed in claim 36, further comprising the steps of forming, after forming said single gate structure of said second transistor, an interlayer insulating film just above said second conductive film of said single gate structure; forming a contact hole in said interlayer insulating film so as to reach said second conductive film of said single gate structure but not to exceed the third insulating film

thereof and forming a wiring layer on said interlayer insulating film, said wiring layer being electrically connected through said contact hole to said second conductive film of said single gate structure.

43. A semiconductor device comprising:

a first transistor having a composite gate structure containing a first conductive film, an insulating film, and a second conductive film; and

a second transistor having a single gate structure containing a third conductive film;

wherein said second conductive film and said third conductive film have substantially the same conductivity;

said third conductive film has a thickness substantially the same as a total of a thickness of said first conductive film, a thickness of said insulating film, and a thickness of said second conductive film; and

said first conductive film has a conductivity different from the conductivity of any of said second and third conductive films.

44. A semiconductor device as claimed in claim 43, wherein said third conductive film contains a multilayer conductive film.

45. A semiconductor device as claimed in claim 44, wherein said first conductive film contains a first silicon film, said second conductive film contains a second silicon film, and said third conductive film contains third and fourth silicon films.

46. A semiconductor device as claimed in claim 45, wherein said first silicon film contains an impurity at an impurity concentration of 1×10^{18} to 1×10^{19} atoms/cm^3, and each of said second, third, and fourth silicon films contains an impurity at an impurity concentration of 1×10^{20} to 1×10^{21} atoms/cm^3.

47. A semiconductor device as claimed in claim 43, wherein said insulating film contains a nitride film.

48. A semiconductor device as claimed in claim 43, wherein said insulating film is a multilayer insulating film containing at least an oxide film and a nitride film.

49. A semiconductor device as claimed in claim 43, wherein said first transistor is a nonvolatile semiconductor memory element, and said second transistor is an MOS transistor.

50. A semiconductor device as claimed in claim 43, wherein said third conductive film contains a lamination of at least a fourth conductive layer and a fifth conductive layer;

said fourth conductive film is facing to said fifth conductive film with an insulating film interposed therebetween in an active region where said second transistor is formed; and

the lamination of the fourth conductive film and the fifth conductive film of said second transistor extend to an element isolation region adjacent said active region; and said fourth conductive film is in face

to face contact with said fifth conductive film in said element isolation region.

51. A semiconductor device as claimed in claim 43, wherein said third conductive film contains a fourth conductive film and a fifth conductive film formed just on an enter surface of said fourth conductive film.

52. A semiconductor device as claimed in claim 43, wherein said first conductive film contains a first silicon film, said second conductive film contains a second silicon film, and said third conductive film contains third and fourth silicon films.

53. A semiconductor device as claimed in claim 50, wherein said insulating film is formed just above an entire surface of said fourth conductive film and said fifth conductive film is formed just above an entire surface of said insulating film.

54. A semiconductor device as claimed in claim 43, wherein said first conductive film is formed on a second insulating film formed on a surface of a first active region of a semiconductor substrate; said first conductive film, said first-mentioned insulating film and said second conductive film are patterned into a shape of said composite gate structure of said first transistor in said first active region; and said third conductive film is formed on a third insulating film formed on a surface of a second active region of said semiconductor substrate and patterned to a shape of said single gate structure of said second transistor in said second active region; and

said semiconductor device further comprises:

drain/source regions of said first transistor formed in said first active region at both sides of said first conductive film, which has been patterned into the shape of said composite gate structure of said first transistor; and

drain/source regions of said second transistor formed in said second active region at both sides of said third conductive film, which has been patterned into the shape of said single gate structure of said second transistor.

55. A semiconductor device comprising:

a first transistor having a composite gate structure containing a lamination of a first conductive film, an insulating film formed on said first conductive film, and a second conductive film having a conductivity different from that of said first conductive film and formed on said insulating film; and

a second transistor having a single gate structure containing a third conductive film having a conductivity substantially the same as that of said second conductive film, and a thickness substantially the same as a total of film thickness of said first conductive film and a film thickness of said second conductive film.

56. A semiconductor device as claimed in claim 55, wherein said third conductive film contains a first silicon film and a second silicon film.

57. A semiconductor device as claimed in claim 55, wherein said insulating film contains a nitride film.

58. A semiconductor device as claimed in claim 55, wherein said insulating film is a multilayer insulating film containing at least a nitride film and an oxide film.

59. A semiconductor device as claimed in claim 55, wherein said third conductive film contains at least two layers of a fourth conductive film and a fifth conductive film;

said fourth conductive film is laminated on said fifth conductive film with an insulating film interposed therebetween in an active region where said second transistor is formed; and

a lamination of the fourth conductive film and the fifth conductive film of said second transistor extends to an element isolation region adjacent said active region and said fourth and fifth conductive films are in face-to-face contact with each other in said element isolation region.

60. A semiconductor device as claimed in claim 55, wherein said first conductive film is formed on a second insulating film formed on a surface of a first active region of a semiconductor substrate; said first conductive film, said first-mentioned insulating film and said second conductive film are patterned into a shape of said composite gate structure of said first transistor in said first active region; and said third conductive film is

formed on a third insulating film formed on a surface of a second active region of said semiconductor substrate and patterned into a shape of said single gate structure of said second transistor in said second active region; and said semiconductor device further comprises:

drain/source regions of said first transistor formed in said first active region at both sides of said first conductive film, which has been patterned to the shape of said composite gate structure of said first transistor; and

drain/source regions of said second transistor formed in said second active region at both sides of said third conductive film, which has been patterned to the shape of said single gate structure of said second transistor.

61. A semiconductor device as claimed in claim 59, further comprising an interlayer insulating film formed just above at least said fifth conductive film in said active region where said second transistor is formed, a contact hole formed in said interlayer insulating film so as to reach at least said fifth conductive film and not to exceed said insulating film disposed between said fourth and fifth conductive films and a wiring layer formed on said interlayer insulating film and electrically connected through said contact hole to said fifth conductive film.

62. A semiconductor device comprising:

a first transistor having a composite gate

structure containing a lamination of a first conductive film, an insulating film formed on said first conductive film, and a second conductive film having a conductivity different from that of said first conductive film and formed on said insulating film; and

a second transistor having a single gate structure containing a third conductive film having a conductivity substantially the same as that of said second conductive film, and also having substantially the same thickness as a total of a film thickness of said first conductive film, a film thickness of said second conductive film and a film thickness of said insulating film.

63. A semiconductor device as claimed in claim 62, wherein said third conductive film contains a first silicon film and a second silicon film.

64. A semiconductor device as claimed in claim 62, wherein said insulating film contains a nitride film.

65. A semiconductor device as claimed in claim 62, wherein said insulating film is a multilayer insulating film containing at least a nitride film and an oxide film.

66. A semiconductor device as claimed in claim 62, wherein said third conductive film contains at least two layers of a fourth conductive film and a fifth conductive film;

said fourth conductive film is laminated on said fifth conductive film with an insulating film

interposed therebetween in an active region where said second transistor is formed; and

a lamination of the fourth conductive film and the fifth conductive film of said second transistor extends to an element isolation region adjacent said active region; and said fourth and fifth conductive films are in face-to-face contact with each other in said element isolation region.

67. A semiconductor device as claimed in claim 62, wherein said first conductive film is formed on a second insulating film formed on a surface of a first active region of a semiconductor substrate; said first conductive film, said first-mentioned insulating film formed on said first conductive film, and said second conductive film are patterned into a shape of said composite gate structure of said first transistor in said first active region; said third conductive film is formed on a third insulating film formed on a surface of a second active region of said semiconductor substrate and patterned to a shape of said single gate structure of said second transistor in said second active region; and said semiconductor device further comprises:

drain/source regions of said first transistor formed in said first active region at both sides of said first conductive film, which has been patterned to the shape of said composite gate structure of said first transistor; and

drain/source regions of said second transistor

formed in said second active region at both sides of said third conductive film, which has been patterned to the shape of said single gate structure of said second transistor.

68. A method for manufacturing a semiconductor device comprising the steps of:

forming a first insulating film on a surface of an active region of a semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a second insulating film on said first conductive film above at least said active region except for an element isolation region of said semiconductor substrate;

forming a second conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first predetermined concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said first conductive film and said second conductive film to a predetermined shape.

69. A method as claimed in claim 68, wherein said second insulating film includes a nitride film.

70. A method as claimed in claim 68, wherein said second insulating film is a multilayer insulating film containing an oxide film and a nitride film.

71. A method as claimed in claim 68, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

72. A method as claimed in claim 68, wherein said first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3 and said second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

73. A method as claimed in claim 68, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a composite gate structure of a transistor.

74. A method as claimed in claim 68, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a single gate structure of a transistor.

75. A method for manufacturing a semiconductor device comprising the steps of:

forming a first insulating film on a surface of an active region of a semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a second insulating film on said first

conductive film;

forming a second conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first predetermined concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said first conductive film and said second conductive film to a predetermined shape.

76. A method as claimed in claim 75, wherein said patterning step includes a substep of patterning a lamination of said second conductive film, said second insulating film, and said first conductive film to a first predetermined shape in said active region, and patterning a lamination of said second conductive film and said first conductive film into a second predetermined shape in an element isolation region of said semiconductor substrate.

77. A method as claimed in claim 75, wherein said second insulating film includes a nitride film.

78. A method as claimed in claim 75, wherein said second insulating film is a multilayer insulating film containing an oxide film and a nitride film.

79. A method as claimed in claim 75, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

80. A method as claimed in claim 75, wherein said

first impurity concentration is 1×10^{18} to 1×10^{19} atoms/cm^3, and said second impurity concentration is 1×10^{20} to 1×10^{21} atoms/cm^3.

81. A method as claimed in claim 75, wherein

in said patterning step, the lamination of said first conductive film and said second conductive film is patterned in a shape of a composite gate structure of a transistor.

82. A method as claimed in claim 75, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a single gate structure of a transistor.

83. A semiconductor device comprising:

a lamination of a first conductive film and a second conductive film, said lamination extending on an active region and an element isolation region of a semiconductor substrate;

wherein said first conductive film is facing to said second conductive film in said active region with an insulating film interposed therebetween and in face-to-face contact with each other said second conductive region in said element isolation region; and

said lamination is patterned into respective predetermined patterns in said active region and said element isolation region.

84. A semiconductor device as claimed in claim 83, wherein said first conductive film includes a first silicon film and said second conductive film includes a

second silicon film.

85. A semiconductor device as claimed in claim 83, wherein said second insulating film includes a nitride film.

86. A semiconductor device as claimed in claim 83, wherein said second insulating film is a multilayer insulating film containing an oxide film and a nitride film.

87. A semiconductor device as claimed in claim 83, wherein said second conductive film is formed immediately above an entire surface of said first conductive film in said element isolation region.

88. A semiconductor device as claimed in claim 83, wherein said insulating film is formed immediately above said first conductive film and said second conductive film is formed immediately above said insulating film in said active region.

89. A semiconductor device as claimed in claim 83, wherein an impurity is introduced into said first conductive film at a concentration of 1×10^{18} to 1×10^{19} atoms/cm^3 in said active region, and an impurity is introduced into said second conductive film at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3 in said active region.

90. A semiconductor device as claimed in claim 83, wherein an impurity is introduced at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3 into each of said first conductive film and said second conductive film in said

element isolation region.

91. A semiconductor device as claimed in claim 83, wherein said first conductive film has a conductivity lower than that of said second conductive film in said active region.

92. A semiconductor device as claimed in claim 83, wherein said first conductive film has substantially the same conductivity as that of said second conductive film in said element isolation region.

93. A semiconductor device as claimed in claim 83, wherein said semiconductor device is an MOS transistor.

94. A semiconductor device as claimed in claim 83, wherein a second insulating film is formed on a surface of said active region of said semiconductor substrate; and said first conductive film is formed on said second insulating film; and said semiconductor device further comprises source/drain regions formed at both sides of said first conductive film in said active region.

95. A semiconductor device as claimed in claim 83, further comprising an interlayer insulating film formed over said second conductive film formed above said active region; a contact hole formed in said interlayer insulating film so as to reach said second conductive film but not to exceed said insulating film formed between said first and second conductive films formed in said active region; and a wiring layer formed on said interlayer insulating film and electrically connected through said contact hole to said second conductive film.